



## 8 Bit Latched Input Monolithic D to A Converter

### FEATURES

- Contains DAC with data latch and on-chip reference.
- Guaranteed monotonic over the full operating temperature range
- Single +5V supply
- TTL and 5V CMOS compatible
- 800 ns settling time
- ZN428E-8 Commercial temperature range 0°C to +70°C
- ZN428J-8 Military temperature range -55°C to +125°C

### GENERAL DESCRIPTION

The ZN428 is a Monolithic 8 bit D to A converter with input latches to facilitate updating from a data bus. The latch is transparent when  $\overline{\text{Enable}}$  is LOW and the data is held when  $\overline{\text{Enable}}$  is taken HIGH. The ZN428 also contains a 2.5 volt reference the use of which is pin optional to retain flexibility. An external fixed or varying reference may therefore be substituted.

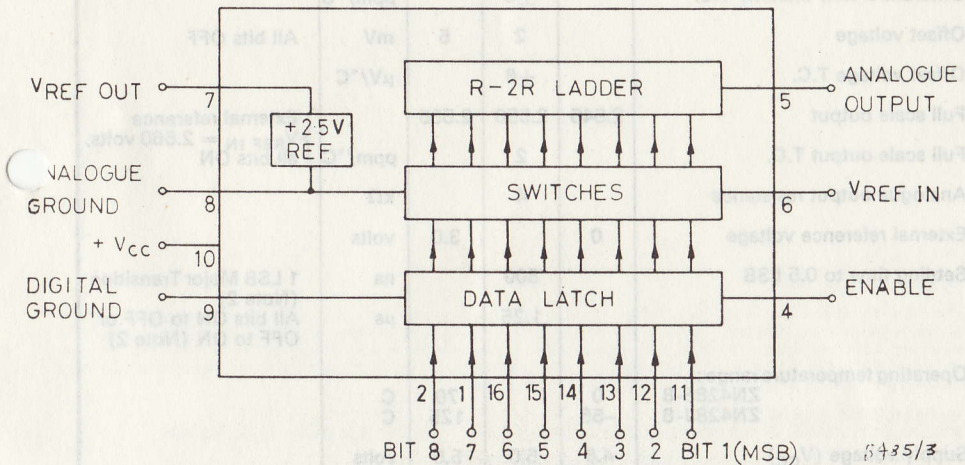


Fig. 1 SYSTEM DIAGRAM

# ZN428E-8/J-8

## ABSOLUTE MAXIMUM RATINGS

Supply voltage $V_{CC}$	.. .. .	+7.0 volts
Max. voltage, logic and $V_{REF}$ input	.. .. .	+ $V_{CC}$
Operating temperature range	.. .. .	0°C to +70°C (ZN428E-8) -55°C to +125°C (ZN428J-8)
Storage temperature range	.. .. .	-55°C to +125°C
Analogue Ground to Digital Ground	.. .. .	±200 mV

## ELECTRICAL CHARACTERISTICS ( $V_{CC} = +5$ volts, $T_{amb} = 25^\circ\text{C}$ unless otherwise specified).

Parameter	Min.	Typ.	Max.	Units	Conditions
<b>Internal Voltage Reference</b>					
Output voltage	2.475	2.550	2.625	volts	} $R_{REF} = 390\Omega$ $C_{REF} = 1\mu\text{F}$
Slope resistance		0.5	2	$\Omega$	
$V_{REFOUT}$ T.C.		50		ppm/°C	
Reference current	4		15	mA	Note 1
<b>D to A Converter</b>					
Linearity error			±0.5	LSB	$2.0\text{V} \leq V_{REFIN} \leq 3.0\text{V}$
Differential non-linearity		±0.5		LSB	
Linearity error T.C.		±3		ppm/°C	
Differential non-linearity T.C.		±6		ppm/°C	
Offset voltage		2	5	mV	All bits OFF
Offset voltage T.C.		±6		$\mu\text{V}/^\circ\text{C}$	
Full scale output	2.545	2.550	2.555		} External reference $V_{REFIN} = 2.560$ volts, all bits ON
Full scale output T.C.		2		ppm/°C	
Analogue output resistance		4		k $\Omega$	
External reference voltage	0		3.0	volts	
Settling time to 0.5 LSB		800		ns	1 LSB Major Transition (Note 2) All bits ON to OFF or OFF to ON (Note 2)
		1.25		$\mu\text{s}$	
Operating temperature range:					
ZN428E-8	0		70	C	
ZN428J-8	-55		125	C	
Supply voltage ( $V_{CC}$ )	4.5	5.0	5.5	volts	

Note 1 See REFERENCE, page 4.

Note 2  $R_L = 10\text{M}\Omega$ ,  $C_L = 10\text{pF}$ .

# ZN428E-8/J-8

## ELECTRICAL CHARACTERISTICS (continued)

	Min.	Typ.	Max.	Units	Conditions
Supply current		20	30	mA	Note 3
Power consumption		100		mW	
<b>Logic</b> (over specified operating temperature range)					
High level input voltage	2.0			V	
Low level input voltage			0.8	V	
High level input current			60	$\mu$ A	$V_{IN} = 5.5V$ $V_{CC} = \text{Max.}$
			20	$\mu$ A	
Low level input current			-5	$\mu$ A	$V_{IN} = 0.4V$ $V_{CC} = \text{Max.}$
Enable pulse width	100			ns	
Data set-up time	150			ns	Note 4
Data hold time	10			ns	Note 5

Note 3 All inputs HIGH ( $V_{IH} = 3.5$  volts).

Note 4 Set up time before  $\overline{\text{Enable}}$  goes high.

Note 5 Hold time after  $\overline{\text{Enable}}$  goes high.

### D to A CONVERTER

The converter is of the voltage switching type and uses an R-2R ladder network as shown in Fig. 2. Each 2R element is connected to 0V or  $V_{REF IN}$  by transistor voltage switches specially designed for low offset voltage (<1 millivolt). A binary weighted voltage is produced at the output of the R-2R ladder.

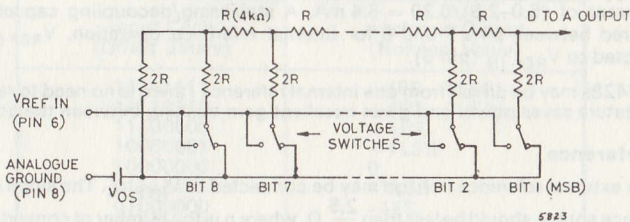


Fig. 2. The R-2R Ladder Network

# ZN428E-8/J-8

$$\text{Analogue Output} = \frac{n}{256} (V_{\text{REF IN}} - V_{\text{OS}}) + V_{\text{OS}}$$

where  $n$  is the digital input to the D to A from the data latch.

$V_{\text{OS}}$  is a small offset voltage produced by the D to A switch currents flowing through the package lead resistance. The value of  $V_{\text{OS}}$  is typically 1 mV. This offset will normally be removed by the setting up procedure (see APPLICATIONS section) and because the offset temperature coefficient is low ( $\pm 6 \mu\text{V}/^\circ\text{C}$ ) the effect on accuracy is negligible.

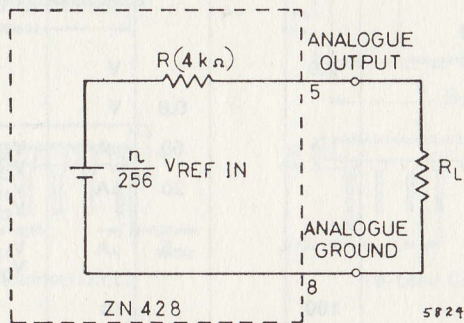


Fig. 3. Analogue Output Equivalent Circuit

Fig. 3 shows an equivalent circuit of the output (ignoring  $V_{\text{OS}}$ ). The output resistance  $R$  has a temperature coefficient of  $+0.2\%$  per  $^\circ\text{C}$ .

The gain drift due to this is  $\frac{0.2R}{R+R_L} \% \text{ per } ^\circ\text{C}$

$R_L$  should be chosen to be as large as possible to make the gain drift small. As an example if  $R_L = 400 \text{ k}\Omega$  then the gain drift due to the T.C. of  $R$  for a  $100^\circ\text{C}$  change in ambient temperature will be less than  $0.2\%$ . Alternatively the ZN428 can be buffered by an amplifier (see APPLICATIONS section).

## REFERENCE

### (a) Internal Reference

The internal reference is an active band gap circuit which is equivalent to a 2.5 volt Zener diode with a very low slope impedance (Fig. 4). A resistor ( $R_{\text{REF}}$ ), should be connected between  $+V_{\text{CC}}$  (pin 10) and pin 7. The recommended value of  $390\Omega$  will supply a nominal reference current of  $(5.0-2.5)/0.39 = 6.4 \text{ mA}$ . A stabilising/decoupling capacitor,  $C_{\text{REF}} = 1 \mu\text{F}$  is required between pins 7 and 8 for internal reference operation,  $V_{\text{REF OUT}}$  (pin 7) being connected to  $V_{\text{REF IN}}$  (pin 6).

Up to five ZN428s may be driven from one internal reference (there is no need to reduce  $R_{\text{REF}}$ ) This useful feature saves power and gives excellent gain tracking between the converters.

### (b) External Reference

If required an external reference voltage may be connected to  $V_{\text{REF IN}}$ . The slope resistance of such a reference source should be less than  $\frac{2.5}{n} \Omega$ , where  $n$  is the number of converters supplied.

$V_{\text{REF IN}}$  can be varied from 0 to  $+3$  volts for ratiometric operation. The ZN428 is guaranteed monotonic for  $V_{\text{REF IN}}$  above 2 volts.

# ZN428E-8/J-8

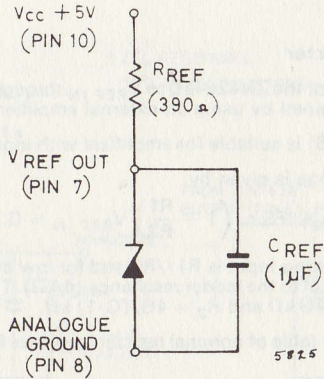


Fig. 4. Internal Voltage Reference

## LOGIC

Input coding is binary for unipolar operation and offset binary for bipolar operation. When the Enable input is low the data inputs drive the D to A directly. When Enable goes high the input data word is held in the data latch.

The equivalent circuit for the data and clock inputs is shown in Fig. 5.

The ZN428 is provided with separate analogue and digital ground connections. The circuit will operate correctly with as much as  $\pm 200$  mV between the two grounds.

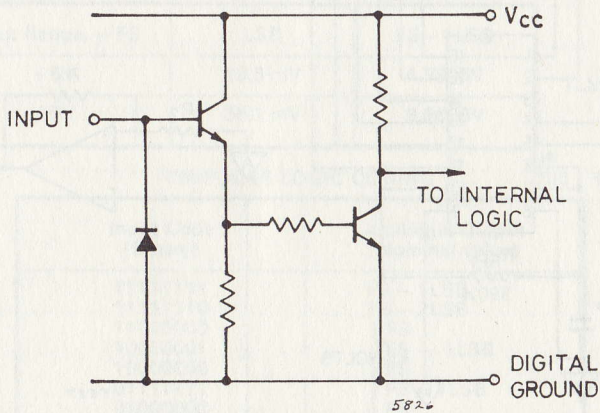


Fig. 5. Equivalent Circuit of All Inputs

# ZN428E-8/J-8

## APPLICATIONS

### (1) Unipolar D to A Converter

The nominal output range of the ZN428 is 0 to  $V_{REF IN}$  through a  $4\text{ k}\Omega$  resistance. Other output ranges can readily be obtained by using an external amplifier.

The general scheme (Fig. 6) is suitable for amplifiers with input bias currents less than  $1.5\ \mu\text{A}$ .

The resulting full scale range is given by

$$V_{OUT FS} = \left(1 - \frac{R_1}{R_2}\right) V_{REF IN} = G \cdot V_{REF IN}$$

The impedance at the inverting input is  $R_1//R_2$  and for low drift with temperature this parallel combination should be equal to the ladder resistance ( $4\text{ k}\Omega$ ). The required nominal values of  $R_1$  and  $R_2$  are given by  $R_1 = 4G\text{ k}\Omega$  and  $R_2 = 4G/(G-1)\text{ k}\Omega$ .

Using these relationships a table of nominal resistance values for  $R_1$  and  $R_2$  can be constructed for  $V_{REF IN} = 2.5\text{ volts}$ .

Output Range	G	$R_1$	$R_2$
+5V	2	$8\text{ k}\Omega$	$8\text{ k}\Omega$
+10V	4	$16\text{ k}\Omega$	$5.33\text{ k}\Omega$

For gain setting  $R_1$  is adjusted about its nominal value. Practical circuit realisations (including amplifier stabilising components) for +5V and +10V output ranges are given in Fig. 7. Settling time for a major transition is  $1.5\ \mu\text{s}$  typical.

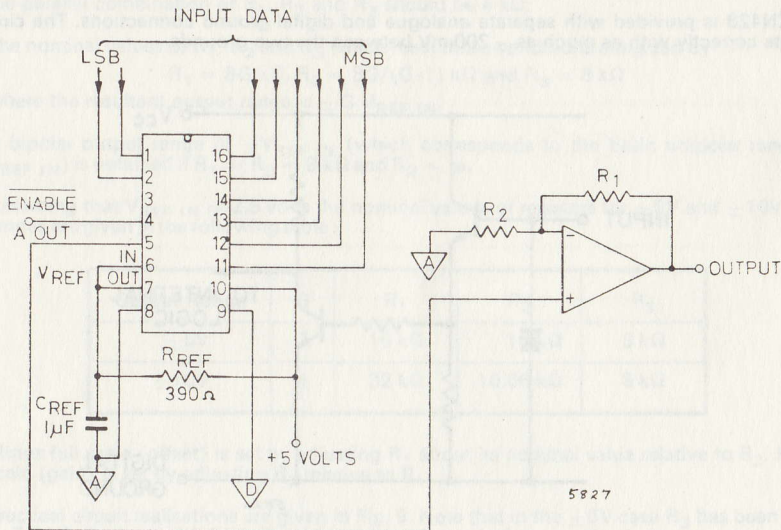


Fig. 6. Unipolar operation – Basic Circuit

# ZN428E-8/J-8

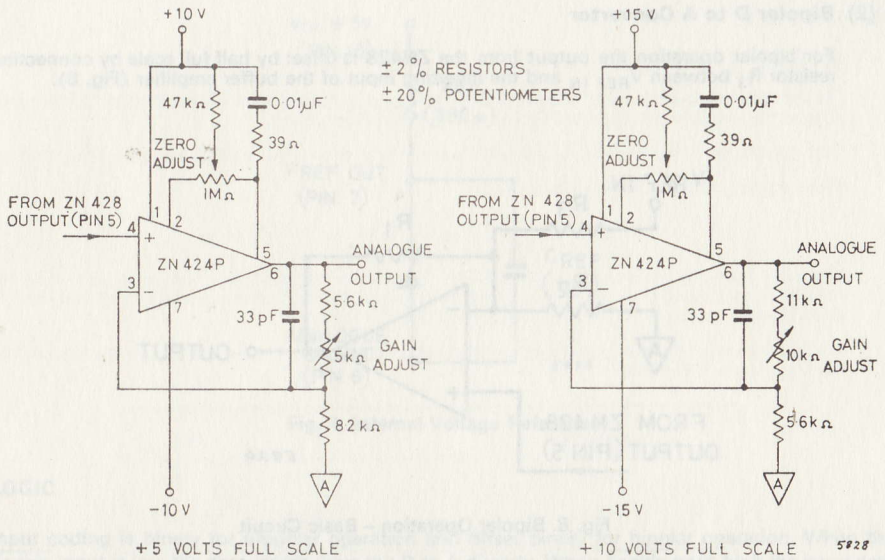


Fig. 7. Unipolar Operation – Component Values

### UNIPOLAR ADJUSTMENT PROCEDURE

- (i) Set all bits to OFF (low) with  $\overline{\text{Enable}}$  low and adjust zero until  $V_{\text{OUT}} = 0.0000\text{V}$ .
- (ii) Set all bits ON (high) and adjust gain until  $V_{\text{OUT}} = \text{FS} - 1\text{LSB}$ .

### UNIPOLAR SETTING UP POINTS

Output Range, +FS	LSB	FS - 1LSB
+5V	19.5 mV	4.9805V
+10V	39.1 mV	9.9609V

$$1\text{LSB} = \frac{\text{FS}}{256}$$

### UNIPOLAR LOGIC CODING

Input Code (Binary)	Analogue Output (Nominal value)
11111111	FS - 1LSB
11111110	FS - 2LSB
11000000	$\frac{3}{4}$ FS
10000001	$\frac{1}{2}$ FS + 1LSB
10000000	FS
01111111	$\frac{1}{2}$ FS - 1LSB
01000000	$\frac{1}{4}$ FS
00000001	1LSB
00000000	0

# ZN428E-8/J-8

## (2) Bipolar D to A Converter

For bipolar operation the output from the ZN428 is offset by half full scale by connecting a resistor  $R_3$  between  $V_{REF IN}$  and the inverting input of the buffer amplifier (Fig. 8).

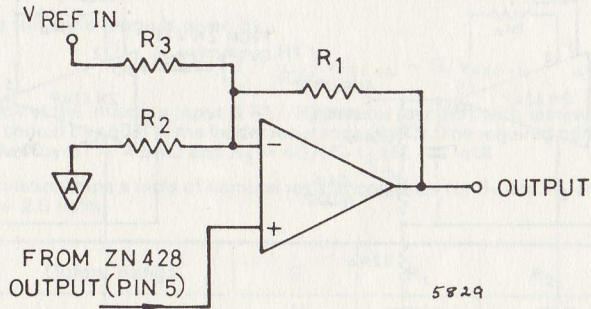


Fig. 8. Bipolar Operation – Basic Circuit

When the digital input to the ZN428 is zero the analogue output is zero and the amplifier output should be -Full scale. An input of all ones to the D to A will give a ZN428 output of  $V_{REF IN}$  and the amplifier output required is + Full scale. Also, to match the ladder resistance the parallel combination of  $R_1$ ,  $R_2$  and  $R_3$  should be  $4\text{ k}\Omega$ .

The nominal values of  $R_1$ ,  $R_2$  and  $R_3$  which meet these conditions are given by

$$R_1 = 8G\text{ k}\Omega, R_2 = 8G/(G-1)\text{ k}\Omega \text{ and } R_3 = 8\text{ k}\Omega$$

where the resultant output range is  $\pm G V_{REF IN}$ .

A bipolar output range of  $\pm V_{REF IN}$  (which corresponds to the basic unipolar range 0 to  $V_{REF IN}$ ) is obtained if  $R_1 = R_3 = 8\text{ k}\Omega$  and  $R_2 = \infty$ .

Assuming that  $V_{REF IN} = 2.5$  volts the nominal values of resistors for  $\pm 5V$  and  $\pm 10V$  output ranges are given in the following table:

Output Range	G	$R_1$	$R_2$	$R_3$
$\pm 5V$	2	16 k $\Omega$	16 k $\Omega$	8 k $\Omega$
$\pm 10V$	4	32 k $\Omega$	10.66 k $\Omega$	8 k $\Omega$

Minus full scale (offset) is set by adjusting  $R_1$  about its nominal value relative to  $R_3$ . Plus full scale (gain) is set by adjusting  $R_2$  relative to  $R_1$ .

Practical circuit realisations are given in Fig. 9. Note that in the  $\pm 5V$  case  $R_3$  has been chosen as  $7.5\text{ k}\Omega$  (instead of  $8.2\text{ k}\Omega$ ) to get a more symmetrical range of adjustment using standard potentiometers. Settling time for a major transition is  $1.5\text{ }\mu\text{s}$  typical.



# ZN428E-8/J-8

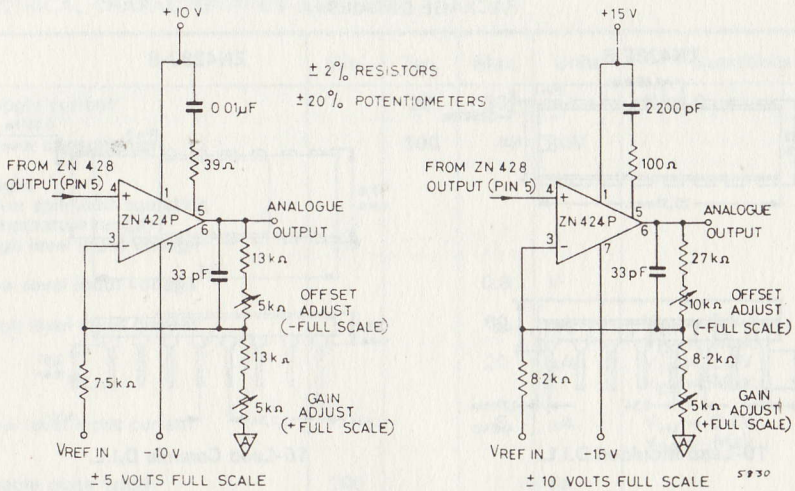


Fig. 9. Bipolar Operation – Component Values

### Bipolar Adjustment Procedure

- (1) Set all bits to OFF (low) with  $\overline{\text{Enable}}$  low and adjust offset until the amplifier output reads -Full Scale.
- (2) Set all bits ON (high) and adjust gain until the amplifier output reads + (Full Scale - 1LSB).

### BIPOLAR SETTING UP POINTS

Input Range, ±FS	LSB	-FS	+(FS-1LSB)
±5V	39.1 mV	-5.0000V	+4.9609V
±10V	78.1 mV	-10.0000V	+9.9219V

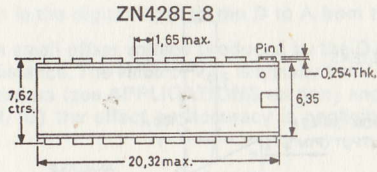
$$1 \text{ LSB} = \frac{2\text{FS}}{256}$$

### BIPOLAR LOGIC CODING

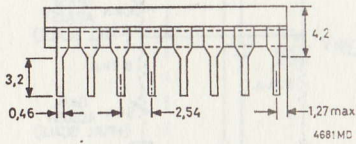
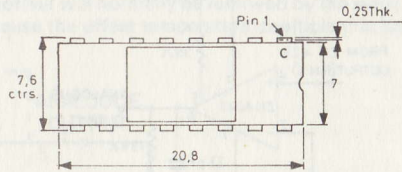
Input Code (Offset Binary)	Analogue Output (Nominal Value)
11111111	+(FS - 1LSB)
11111110	+(FS - 2LSB)
11000000	+½FS
10000001	+1LSB
10000000	0
01111111	-1LSB
01000000	-½FS
00000001	-(FS - 1LSB)
00000000	-FS

# ZN428E-8/J-8

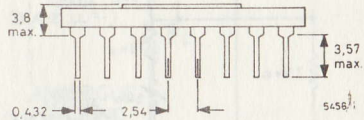
## PACKAGE DETAILS



ZN428J-8



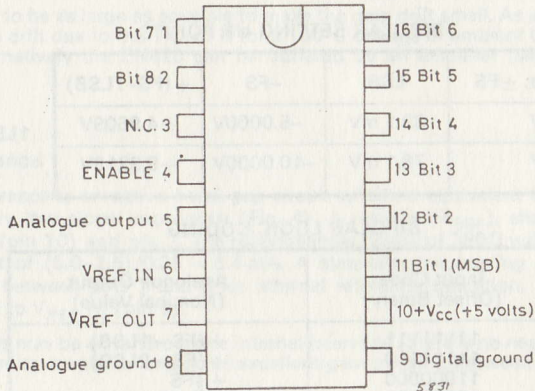
16-Lead Moulded D.I.L.



16-Lead Ceramic D.I.L.

Dimensions in millimetres

## PIN CONNECTIONS



# NOTES

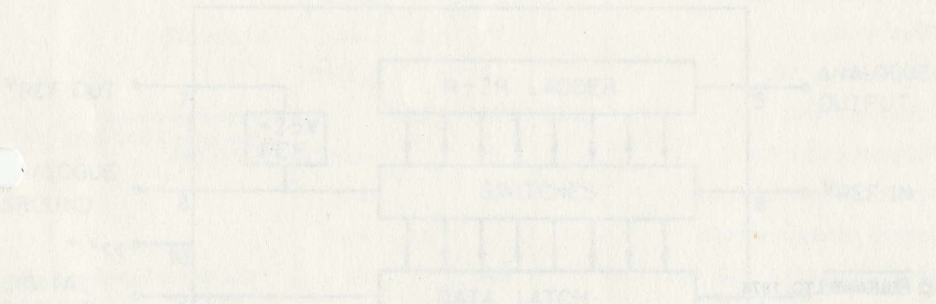
## 8 Bit Latched Input Monolithic D to A Converter

### FEATURES

- Contains DAC with data latch and on-chip reference.
- Operating over the full operating temperature range.
- Single  $\pm 5V$  supply.
- TTL and E<sub>2</sub> CMOS compatible.
- 200 ns settling time.
- Package B - Commercial temperature range - 0°C to +70°C
- Package S - Military temperature range - 55°C to +125°C

### GENERAL DESCRIPTION

The ZN428 is a Monolithic 8 bit D to A converter with input latches to facilitate operation from a data bus. The latch is transparent when  $\overline{LATCH}$  is high and the data is latched when  $\overline{LATCH}$  is taken HIGH. The ZN428 also contains a 2.5 volt reference which is taken in relation to the input of the DAC. An external feedback network may therefore be used to adjust the transfer characteristics.



The ZN428 is a monolithic 8 bit D to A converter with input latches to facilitate operation from a data bus. The latch is transparent when LATCH is high and the data is latched when LATCH is taken HIGH. The ZN428 also contains a 2.5 volt reference which is taken in relation to the input of the DAC. An external feedback network may therefore be used to adjust the transfer characteristics.

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# ZN428E-8/J-8

83108

## ABSOLUTE MAXIMUM RATINGS

Supply voltage $V_{CC}$	+7.5 volts
Max. voltage logic and $V_{CC}$ input	$-V_{CC}$
Operating temperature range	0°C to +75°C (ZN428E-8) -55°C to +125°C (ZN428E-8J)
Storage temperature range	-55°C to +125°C
Analogue Ground to Digital Ground	-100 mV

## ELECTRICAL CHARACTERISTICS ( $V_{CC} = +5$ V, $T_{amb} = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Min.	Typ.	Max.	Units	Conditions
Internal Voltage Reference					
Output voltage	2.475	2.500	2.525	volts	$I_{REF} = 2000$ $C_{REF} = 1 \mu\text{F}$
Stops resistance		0.2	2	$\Omega$	
Voltage T.C.		30		ppm/°C	
Reference current	4		15	mA	Pin 1
D to A Converter Linearity error			±0.5	LSB	2.0V $V_{REF} = 4.30V$
Differential non-linearity		±0.5		LSB	
Density error T.C.		±3		ppm/°C	
Differential non-linearity T.C.		±6		ppm/°C	
Offset voltage		2	8	mV	All bits OFF
Offset voltage T.C.		±6		mV/°C	
Full scale output	2.545	2.550	2.555		External reference $V_{REF} = 2.550$ volts All bits ON
Full scale output T.C.		2		ppm/°C	
Analogue output resistance		4		$\Omega$	
External reference voltage	0		2.0	volts	

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